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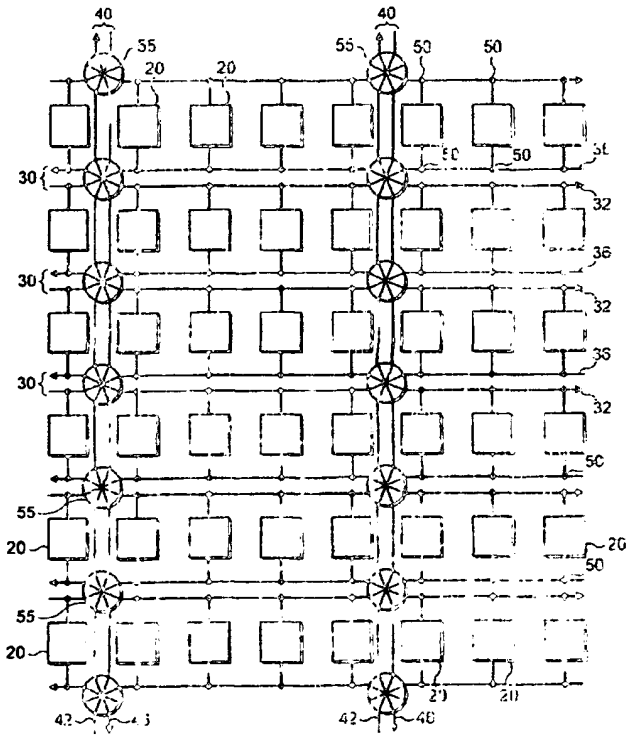

(57) Abstract: There is described a processor architecture having a plurality of processing elements, each element having at least one input port and at least one output port, each port having at least a data bus and a valid data signal line; and a bus structure which contains a plurality of switches which are arranged so as to allow an output port of any first processing element to be connected to the input port of any second processing element for a time interval, in which each processing element is enabled to set a value on the valid data signal line of its output port to a first logic state when the associated data bus contains a transfer value, and to a second logic state when the data bus does not contain a transfer value, and in which each processing element is further enabled to enter a waiting state for a predetermined time interval when the value on the valid data signal line of the associated input port is in the second logic state. This reduces the power consumption of the device.

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PROCESSOR ARCHITECTURE

This invention relates to a processor architecture, and in particular to an architecture which can be used in a wide range of devices, such as communications devices operating under different standards.

In the field of digital communications, there has been a trend to move as many functions as possible from the analogue domain into the digital domain. This has been driven by the benefits of increased reliability, ease of manufacture and better performance achievable from digital circuits, as well as the ever decreasing cost of CMOS integrated circuits. Today, the Analogue-Digital and Digital-Analogue Converters (ADC's and DAC's) have been pushed almost as near to the antenna as possible, with digital processing now accounting for parts of the Intermediate Frequency (IF) processing as well as baseband processing.

At the same time, there has been a vast improvement in the capability of microprocessors, and much of the processing for many narrowband communications systems is now performed in software, an example being the prevalence of software modems in PC's and consumer electronics equipment, partly because a general purpose processor with sufficient processing power is already present in the system. In the field of wireless communications there is extensive research in the field of software radio the physical layers of broadband communications systems require vast amounts of processing power and the ability to implement a true software radio for third generation (3G) mobile communications, for example, is beyond the capability of today's DSP processors, even when they are dedicated to the task.

Despite this, there has never been a time when there has been more need for software radio. When second generation (2G) mobile phones were introduced, their operation was limited to a particular country or region. Also, the major market was business users and a premium could be commanded for handsets. Today, despite diverse 2G standards in the USA and different frequency bands, regional and international roaming is available and handset manufacturers are selling dual and triple band phones which are manufactured in their tens of millions. After years of attempts to make an international standard for 3G mobile the situation has now arisen where there are three different air interfaces, with the one due to replace GSM (UMTS) having both Frequency and Time Division Duplex (FDD and TDD) options. Additionally, particularly in the USA, 3G systems must be capable of supporting a number of legacy 2G systems.

Although a number of DSP processors are currently being developed that may be able to address the computational requirements of a 3G air interface, none of these show promise of being able to meet the requirements of a handset without the use of a number of hardware peripherals. The reasons for this are power and cost and size. All three are interrelated and controlled by the following factors:

1. The need for memory. Classical processor architectures require memory to store both the program and data which is being processed. Even in parallel Very Long Instruction Word (VLIW) or Single Instruction Multiple Data (SIMD) architectures, the entire processor is devoted to one task at a time (eg: a filter, FFT or Viterbi decoding), with memory required to hold intermediate results between the tasks. In addition, fast local instruction and data caches are required. Altogether, this increases the size and cost

of the solution, as well as dissipating power. In hard-wired architectures, data is usually transferred directly from one functional block to another, with each block performing DSP functions on the data as it passes through, thus minimising the amount of memory required.

2. Data bandwidth. In hard-wired solutions, all data is held locally, if necessary in small local RAM's within functional blocks. Some transceivers may contains several dozen small RAM's, and although the data bandwidth required by each RAM may be relatively small the overall data bandwidth can be vast. When the same functions are implemented in software running on a processor, the same global memories are used for all data and the required data bandwidth is enormous. Solutions to this problem usually involve the introduction of local memories in a multi-processor array, but the duplication of data on different processors and the task of transferring data between processors via Direct Memory Access (DMA) mean that the power dissipation is, if anything, increased, as is silicon area and consequently cost.

3. The need for raw processing power. In today's DSP processors, improvements in processing throughput are achieved by a combination of smaller manufacturing process geometries, pipelining and the addition of more execution units (e.g. arithmetic logic units and multiplier-accumulators). Improvements in manufacturing processes are open to all solutions, and so are not a particular advantage for conventional DSP processors. The other two methods both come with considerable overheads in increased area and power, not merely because of the extra hardware which provides the performance improvement, but because of the consequential increases in control complexity.

The processor architecture of the present

invention falls under the broad category of what are sometimes referred to as dataflow architectures, but with some key differences which address the needs of software. In fact, the invention provides a solution which is more akin to a hard-wired architecture than a DSP processor, with consequential size and power advantages. It consists of an array of processor and memory elements connected by switch matrices.

According to the present invention, there is provided a processor architecture comprising:

a plurality of processing elements, each element having at least one input port and at least one output port, each port having at least a data bus and a valid data signal line; and

a bus structure which contains a plurality of switches which are arranged so as to allow an output port of any first processing element to be connected to the input port of any second processing element for a time interval,

each processing element being enabled to set a value on the valid signal data signal line of its output port to a first logic state when the associated data bus contains a transfer value, and to a second logic state when the data bus does not contain a transfer value:

each processing element being further enabled to enter a waiting state for a predetermined time interval when the value on the valid signal data signal line of the associated input port is in the second logic state.

The waiting state is, for example, a low power sleep mode.

This has the advantage that the power consumption of the device can be reduced when there is no data to be processed.

Preferably, the processing elements are programmable in such a way as to set a predetermined time

internal

Preferably, the processing element is further enabled to load data from the data bus of its input port when the value of the valid signal data signal line of the associated input port is in the first logic state.

Preferably, the front port of each processing element is connected to the bus structure at a location in front of a location at which the corresponding output port is connected to the bus structure, in the direction of signal flow, such that, during a transfer time period, the second processing element may set a second transfer value on the bus structure.

This achieves a further power saving in that, when data is not being transferred across a section of the bus structure, it does not need to be charged and discharged unnecessarily.

Preferably, the processing elements include memory elements for storing received data, and/or processing elements including Arithmetic Logic Units and Multiplier Accumulators.

Preferably, each processing element has:

a first input for receiving data from a first bus;

a first output for transferring data to the first bus;

a second input for receiving data from a second bus; and

a second output for transferring data to the second bus.

The architecture of the preferred embodiment allows flexible data routing between array elements using a switch matrix. This means that the device is able to run many diverse algorithms required by a software radio concurrently, without having to reconfigure the array.

Reference will now be made, by way of example, to the accompanying drawings, in which:

Figure 1 is a schematic representation of a section of a processor, illustrating the architecture in accordance with the invention;

Figure 2 is an enlarged representation of a part of the architecture of Figure 1;

Figure 3 is an enlarged representation of another part of the architecture of Figure 1;

Figure 4 is an enlarged representation of another part of the architecture of Figure 1;

Figure 5 shows the illumination of elements in a typical array in accordance with the invention;

Figure 6 shows a first array element in the architecture of Figure 1;

Figure 7 shows a second array element in the architecture of Figure 1;

Figure 8 shows a first connection of the array element of Figure 7 in the array according to the invention;

Figure 9 shows a second connection of the array element of Figure 7 in the array according to the invention;

Figure 10 shows a third array element in the architecture of Figure 1;

Figure 11 shows a fourth array element in the architecture of Figure 1;

Figure 12 shows the format of data transferred between array elements; and

Figure 13 is a timing diagram illustrating the flow of data between array elements.

Figure 1 shows a part of the structure of a processor architecture 10. The device is made up of an array of elements 20 which are interconnected by buses and switches.

The architecture includes first bus pairs 30, shown running horizontally in Figure 1, each pair including a respective first bus 32 carrying data from left to right in Figure 1 and a respective second bus 36 carrying data from right to left.

The architecture also includes second bus pairs 40, shown running vertically in Figure 1, each pair including a respective third bus 42 shown carrying data upwards in Figure 1 and a respective fourth bus 46 shown carrying data downwards in Figure 1.

In Figure 1, each diamond connection 50 represents a switch, which connects an array element 20 to a respective bus 32, 36. The array further includes a switch matrix 55 at each intersection of a first and second bus pair 30, 40.

The data buses are described herein as 64-bit buses, but for some application areas it is likely that 32-bit buses will suffice. Each array element can be designed to be any one of the following:

an execution array element which contains an Arithmetic Logic Unit (ALU) or Multiplier Accumulator (MAC).

a memory array element, containing a RAM;

an interface array element which connects the processor to an external device, or

a switch control array element, which controls the operation of at least one switch matrix 55.

Each of these will be described in more detail below.

Figure 2 is an enlarged view of a part of the architecture of Figure 1, showing six array elements, 20A-20F. Each array element is connected to two 64-bit buses, 32, 36, which carry data in opposite directions. After every four array elements (as shown in Figure 1), the horizontal buses are connected to two vertical buses, 42, 46, one carrying up and the other

down. The choice of bit width and vertical bus pitch is not fundamental to the architecture but these dimensions are presently preferred.

Each switch element 5 is a 2:1 multiplexer, controllable such that either of its two inputs can be made to appear on its output. Thus output data from an array element can be transferred onto a bus, and/or data already on the bus can be allowed to pass.

The switch matrix 5a includes four 4:1 multiplexers 501, 502, 503 and 504, which are each controllable such that any one of their inputs can appear at their output.

The inputs of multiplexer 501 are connected to input connections 32a, 36a and 42a on buses 32, 36, 42 respectively, and to ground. The output of multiplexer 501 is connected to bus 42.

The inputs of multiplexer 502 are connected to input connections 32a, 36a and 46a on buses 32, 36, 46 respectively, and to ground. The output of multiplexer 502 is connected to bus 46.

The inputs of multiplexer 503 are connected to input connections 32a, 36a, 42a and 46a on buses 32, 36, 42 and 46 respectively. The output of multiplexer 503 is connected to bus 36.

The inputs of multiplexer 504 are connected to input connections 32a, 36a, 42a and 46a on buses 32, 36, 42 and 46 respectively. The output of multiplexer 504 is connected to bus 32.

Thus, in the switch matrix 5a, the input of any bus can be used as the source for data on the output of any bus, except that it is not possible to select the down-bus (i.e. the one extending from the top of the diagram in Figure 2, namely the fourth bus 46) as the source for the up bus (that is, the third bus 42), and, similarly, it is not possible to select the up bus (the third bus 42) as the source of the down bus (the fourth

bus 44.

[illegible] exceptions [illegible] which are not useful in practice. Likewise, however, it is useful to have the left bus as a potential source for the right bus, and vice versa, for example when routing data from array element 20B to array element 20E.

As mentioned above, one of the inputs of each of the multiplexers 501, 502 is connected to ground. That is, each of the 64 bus lines is connected to the value 0. This is used as part of a power reduction method, which will be described further below.

Each of the multiplexers 501, 502, 503, 504 can be controlled by signals on two control lines. That is, a two-bit control signal can determine which of the four inputs to a multiplexer appears on its output.

Figure 5 is a view of the top-left hand corner of the array of Figure 1, showing the structure of a switch matrix 56 which is used when there is no input connection to a left-right bus 42 and of a switch matrix 57 which is used when there is no input connection to a left-right bus 42 or to a bus 46 running down.

The switch matrix 56 includes three 4:1 multiplexers 505, 506, 507, while the switch matrix 57 includes three 4:1 multiplexers 508, 509, 510. Compared to a switch matrix in the middle of the array, the number of input buses to multiplexers 505, 508 and 509 is reduced by one because there is no input bus entering from the left. Similarly, there is no input bus entering from the [illegible] as an input to multiplexer 510, but in this case the input bus which has been released has been numbered 63. This is also the case for multiplexer 511, but in this case there is no input bus entering from the [illegible] either of the multiplexers has only three input buses.

Before the [illegible] of the array, no input buses

from the top or the left are available for multiplexer 506, which only has two inputs. Equivalent arrangements will be apparent for the bottom left, top-right and bottom-right corners of the array.

Figure 4 is a view of part of the top edge of the array of Figure 1, showing the structure of a switch matrix 58 which is used when there is no input connection to a bus 46 running down.

The switch matrix 58 includes two 4:1 multiplexers 511, 512. The inputs of available input buses to multiplexers 511 and 512 are connected by bus, but, in the case of multiplexer 511, one of the input buses has been replaced by the value zero. An equivalent structure for multiplexers on the bottom edge of the array is apparent.

Data transfer can be regarded as having three stages. Firstly, an array element puts the data on the appropriate output.

Secondly, multiplexers in the appropriate switch matrix or switch matrices are activated to make the necessary connections.

Thirdly, the destination array element loads the data.

Each of these events is controlled by a separate array element: the first and third by the source and destination array elements respectively, and the second by special switch control array elements. These are embedded into the array at regular intervals and are connected by control lines to all the multiplexers in the switch matrices which they control. Each array element controls the multiplexers immediately adjacent to its outputs, with the control being performed separately on individual 16-bit fields. This allows several array elements to output data onto a bus at the same time, provided they are on different fields of the bus. Use is specifically made of this feature

such as Add-Compare-Select (ACS) in the Viterbi Algorithm, switching at intersection nodes of horizontal and vertical buses is performed on the entire 64-bit bus and its associated control signals.

Clearly, the three operations of source, switching and loading, although performed independently, need to be synchronised. This is achieved by restricting all data transfer operations to a series of predetermined cycles, which are fixed at the time when the program is compiled and mapped onto the array. In a general purpose processor this restriction would be onerous, but it is actually helpful for many applications of the present invention.

As mentioned previously, there are a number of types of array element, but they all must conform to three basic rules.

Firstly, they must have input and output ports which connect to the left and right buses of the array.

Secondly, they must run a program which is synchronised to the transfer cycles on the buses to which they are connected. In practice, this usually means that each array element must run a program loop which accesses the buses in a regular pattern which has a duration in clock cycles which is a power of two (e.g. 4, 8, 16 or 32 clock cycles).

Thirdly, they must interpret information which appears on the buses during special control cycles, known as the Array Control Protocol.

A consequence of these rules is that, in the normal course of events, the entire program which an array element executes will be contained in local memory within the array element. In fact, more often than not, the program will contain just one loop. It is possible to reload an array element with new instructions, but this involves stopping the processor and reloading the instruction memory of the array element using the control cycles outlined above. The array

element [illegible] conditions autonomously.

[illegible] is to say, [illegible] of their programs when data arrives.

There are two types of [illegible]: Multiplier Accumulator (MAC) array elements and Arithmetic Logic Unit (ALU) array elements. These must be included in the array [illegible] elements in appropriate [illegible] for the target applications. [illegible] may applications [illegible] proportions, and Figure [illegible] shows an example of an array containing 256 array elements in proportions optimised for a communications transceiver. Figure [illegible] does not show the horizontal buses in the array and the positions of pairs of vertical buses 40 are shown as single lines.

As well as MAC, ALU [illegible] Switch Control array elements, the example array of Figure [illegible] contains three interface array elements 80, 81 and 82. Array elements 80 and 81 are used for data input and output to the analogue portions of the transceiver and array element 82 is the interface to a microprocessor. Each of the four Switch Control array elements 83a to 83d controls the switch [illegible] of the array. For example, Switch Control array element 83a controls the switches [illegible] the horizontal buses connected to the [illegible] array elements, 84.

Figure [illegible] shows the [illegible] of a Switch Control array [illegible] controller 94 and RAM 95, together with means of loading the RAM using the Array Control Protocol described below [illegible] RAM. Data is loaded into the RAM from either the left bus 32 or right bus [illegible] Control array

element is connected by the multiplexers 91 and 64-bit registers 93.

When the S[illegible] C[illegible] array element is set into its normal operating mode by means of Table signal 98, the address of RAM 95 is first set to zero and the first 160-bit word is read from and loaded into register 96. On each subsequent clock cycle, the RAM address is incremented and a new 160-bit word is loaded into register 96, until the address reaches 127 at which point it is reset to zero again and the process is repeated. The outputs of register 96 are applied directly to the select inputs of the 2:1 multiplexers in the switch matrices 55 (figures 3 and 5), so in this way all the switch matrices are controlled in a cyclical pattern lasting for 128 clock cycles. As previously noted, most areas of the array transfer data in cyclical patterns of a duration less than 128 clock cycles, but these are accommodated by repeating them within the 128 cycle pattern.

ALU and MAC array elements have the same interfaces to the array, differing only in the type of execution unit and associated instructions. Figure 7 shows an ALU array element, which will be used to describe these interfaces to the array.

Referring to Figure 7, three 64-bit registers, each formed from four 16-bit sub-registers 111a-121d, 121e-121h and 121i-121l can be connected to either of left bus 32 or right bus 36 by switch multiplexers 120, thus allowing them to be loaded from either bus. In response to instructions read from instruction store 123 and decoded in instruction decoder 125, any one 64-bit register can be connected to the left or right bus during one clock cycle and any combination of sub-registers loaded. [illegible] instruction may cause the 16-bit sub-registers 121a and 121e of 64-bit register 121a-121l to be loaded with the 16 bits in bits

31:0 of left bus 12. Further instructions may cause data in the registers to be manipulated by the ALU 125 and stored back into the same or different registers 121, and still further instructions may output the contents of these registers onto the left and right buses via multiplexer 126 and switch box 51. In the preferred embodiment, during the same clock cycle one 16-bit register may be used to load data from an array bus, data from another may be enabled onto another array bus and ALU operations may be performed on the contents of registers, these tasks being accomplished by using separate fields of the instruction words.

Figure 8 shows the contents of a switch box 51 in Figure 7. BUSIN 131 and BUSOUT 132 are 16-bit segments of a left bus 26 or a right bus 31. Control signals EN[3:0] 130 and SEL[3:0] 133 are both sourced by instruction decode block 123 in Figure 7. Using these signals, any 16-bit field of BUSOUT may be set to be equal to BUSIN, the output bus of the array element or zero.

Figure 9 illustrates how, [illegible], the [illegible] signal (described below) associated with the data on the bus can be allowed to pass along the bus or be set by the array element.

Figure 10 shows the preferred embodiment of a Memory array element. This has many of the same features of the ALU array element described above, but in addition has RAMs 143 connected to registers 140, 141 and 142 via multiplexers [illegible]. 16-bit sub-registers R0 to R3 of 64-bit register 140 are used for data input to the RAMs, 16-bit [illegible] register 141 are used for the address input to the RAMs and 16-bit sub-registers [illegible] of 64-bit register 142 are used for the data [illegible]. Both address and data may be [illegible] using the ALU under the control of the instruction [illegible] the

case of the ALU array elements, with the addresses of loading data from the left and right buses 32 and 36 is also performed in exactly the same manner. The instructions stored in instruction store 14[illegible] and decoded in instruction decode unit 145 have an additional field compared to the equivalent ones of the ALU array elements. This additional field is used to control the reading of data from the left and writing of data to the right, these operations being performed in the same cycle as array accesses and ALU operations.

Referring to Figure 11, it can be seen that the addresses for the RAM may be calculated within the Memory array element using the internal ALU and loaded into the sub-registers of the [illegible] register [illegible]. Alternatively, addresses may be provided over the array buses from another array element and loaded directly into register [illegible].

In the example array of Figure [illegible], memory array elements hold all the data [illegible] by the execution array elements and there is no external global memory. However, it will be clear that if a given application requires a large amount of storage, access to external memory can be provided using appropriate Interface array elements. Furthermore, instructions which form the programs of the array elements are not generally stored in memory array elements, but reside entirely in the instruction stores of the array elements. Instructions are loaded into the instruction stores of the array elements using the Array Control [illegible] [illegible].

Figure [illegible] shows how an [illegible] [illegible] Controller [illegible] [illegible] [illegible] processor architecture [illegible] [illegible].

[illegible] [illegible] ALU [illegible] [illegible] only need to [illegible] data [illegible] [illegible] [illegible] the

purp[illegible] ... setting the ... and to control the ... transfers sampled data onto the ... element controller 152 can ... instruction store ... Memory array elements ... being programmed to ... analogue signal ... register ... configurable ...

The primary source of ... are the Digital to Analogue ... element, which ... elements ... latter ... general purpose ... processing ...

The ... according to ... described. However, ... architecture comes ... and in providing ... common computation-in-memory ... physical layer ... will ... minimise ... architecture ... such as ...

A number of ... with the ...

... the data ... array ...

... is valid ... the

control of power [illegible]

A major [illegible] of the [illegible] is to keep the [illegible] of array [illegible], [illegible] the need for complex [illegible]. The Array Control Protocol (ACP) [illegible] the following:

[illegible] elements when the array is [illegible]

[illegible] array elements

[illegible] array elements during operation

Each array element has a Unique Identifier (UID), which is used to [illegible] Array Control Words (ACWs) [illegible] information between array elements. When the [illegible] of a section of the bus is high [illegible] the data on the bus is an ACW. Figure [illegible] shows the structure of the [illegible] ACW.

When an ACW is put on the section of the bus to which an array element is connected, the array element must examine the [illegible] in low-power sleep mode. If the [illegible] field of the ACW matches the UID of the array element or is equal to a designated broadcast address, the array element must interpret the FUNCTION field of the ACW and perform the required action. In one presently preferred embodiment of the invention, the following FUNCTION fields are defined:

Value	Function	Description
0	Reset	[illegible] to halt [illegible] internal [illegible]

1	Load Program 0	The DATA field contains a program word which must be placed in the first location in the program store of the array element
11	Load Program	The DATA field contains a program word which must be placed in the next location in the program store of the array element
100	Start	The array element must start executing program in program store
101	Stop	The array element must stop executing program in program store
110	Test	Byte test mode
111	Dump	Place data from next location in the program store on the bus

An Array may be generated by any array element, but the array will normally be initiated by element which is defined as the master array element and the master controller will generally be the host. The major function of the Array Control Instructions is to load the program stores of the array elements with the code to be executed. Therefore, a host initialises array elements which loads the program supplied by the host processor. The most likely bus to be the source is PCI.

Unlike most processors, which are instruction driven, the processors of the present invention and its component array elements are data driven. That is, instead of fetching an instruction, array elements execute instructions as a result of receiving data.

Once a program has been loaded into an array element and it has been enabled using the eRT Array Control Word it will begin to execute its instruction sequence. Most instructions which requires

it [illegible] data [illegible] data is present on the bus (signified by the [illegible] signal [illegible] being low) it must stop and [illegible] data [illegible] available. During the time [illegible] stopped [illegible] into [illegible] low power sleep [illegible] array element [illegible] the bus [illegible] specified by a field in the load [illegible] stalled to check if the data has [illegible]

[illegible] example [illegible] demodulator. In a demodulator [illegible] described herein, the demodulator [illegible] samples at a fixed rate which generally [illegible] above the actual [illegible] demodulator will [illegible] in [illegible] samples [illegible] incoming data. [illegible] for an analogue VCO to synchronise [illegible] to the data, but the resampled data [illegible] with respect to the processor system clock and data transfer sequences, creating [illegible] data [illegible] have been expected. (In fact the ADC sample clock need not be synchronised to the processor system clock at all, with synchronisation to the system clock being performed in the ADC interface array element.) Using the data driven processor [illegible] of the present invention, where there is a "gap" in the incoming data, the array elements which are affected [illegible] go to sleep' until data is available.

[illegible] should be noted that because [illegible] data transfers are [illegible] which are defined [illegible] the [illegible] and mapped to the processor, [illegible] at least one of the [illegible] are synchronised.

[illegible] this timing diagram, [illegible] (A and B) are [illegible] successive

transfer [illegible] (BDVAL PER SEQ). In the [illegible] on the fourth [illegible] the second (as shown [illegible] they load being shown [illegible] signals LOADREQ [illegible] LOADREQ [illegible] are the BDVAL signals [illegible] loaded by array elements [illegible] that. Where no data is available [illegible] the BDVAL signal [illegible] in which [illegible] sequence [illegible] for array element B, the [illegible] sleep mode until [illegible] that no data is available for [illegible] array elements does not affect [illegible].

Clearly, if [illegible] receive any data, there will be [illegible] it does not [illegible] through the array. However, the [illegible] particular point [illegible] time the program is written, [illegible] which tend [illegible] naturally [illegible] where data needs to be [illegible] where a block of data has to be accumulated before it is processed means that the entire [illegible] gaps which occur [illegible].

In some cases [illegible] element does not receive [illegible] elements must [illegible] multiple [illegible] from a memory [illegible] as not arrived [illegible] is prevented from sending [illegible] data past the [illegible] memory array element [illegible],

the [illegible] sleep mode

[illegible] BDVAL signal [illegible] to it is [illegible]

[illegible] Every time [illegible] ion, which [illegible] data [illegible], it se[illegible] signals [illegible] Figure 8) [illegible] 52 such that BD[illegible] one clock cycle. [illegible] and SE[illegible] BUSCI[illegible] to [illegible] example, if data [illegible] be transferred [illegible] the bus, then all of [illegible] are set to 1. [illegible] data [illegible] transferred on bits [illegible] of the [illegible] are set to 1, [illegible] are set to 1 if [illegible] data on the other bits of [illegible] same clock cycle. [illegible] example of multiple array elements using the same bus segment to transfer data in the same clock cycle, referring to Figure 2 [illegible] can be seen that array element [illegible] transfer data onto bits [31:0] of bus [illegible] whilst array element 20[illegible] transfers data on bits [illegible] array element [illegible] say.

During the [illegible] the [illegible] in switch [illegible] so that the [illegible] are routed to the [illegible] to Figure [illegible] the destination array [illegible]

instr[illegible] [illegible] 12 [illegible] select the bus on the inputs of the [illegible] register 12[illegible], which is loaded at the end of [illegible] of the B[illegible]AL signal [illegible] load takes place and the array [illegible] for [illegible] number of clock cycles specified as part of the [illegible]AT instruction field. During the time that the [illegible] is waiting, the only activity in the array element is the execution control [illegible] which [illegible] the wait period [illegible]. When the count reaches zero the [illegible] control unit [illegible] examines the B[illegible] [illegible]es execution to proceed [illegible] off. Because the circuitry [illegible] control unit is very small compared to the rest of the array element, very little power is consumed while the array element is waiting.

As well as the [illegible] instruction described above, all array elements which [illegible] for data transfer also have a [illegible] instruction. This instruction causes the [illegible] examine the BDVA[illegible] signal [illegible] left bus 12 or right bus 1[illegible] and wait for the specified number of clock cycles [illegible] selected [illegible] signal [illegible] data is loaded.

Throughout the above descriptions, reference has been made to methods of reducing power dissipation in the array. These methods [illegible] described in more detail.

[illegible] data transfer [illegible] the array [illegible] lines and [illegible] signals are [illegible] unless necessary. In order to [illegible] state of all [illegible] Switch [illegible] select the [illegible] being

used [illegible] and 502 in Figures [illegible] and [illegible] edges an[illegible] of the [illegible] Figures [illegible] and 4.

[illegible] data is transferred [illegible] bus often not all 64 bits are used. [illegible] as [illegible] above [illegible] is loading [illegible] 0. If the bus had previously [illegible] these bus would have been [illegible], so the [illegible] values [illegible]

[illegible] Figure [illegible] that if data is being transferred from array element [illegible] to array element 20E, [illegible] and further [illegible] were [illegible] along right bus [illegible] which [illegible] 20E, past array element [illegible] and beyond, thus unnecessarily [illegible] or discharging further segments of [illegible] this [illegible] occurring, all array elements [illegible] destinations for data can cause [illegible] their output switch boxes 51 to be set so that data further along the bus is set to 0 (and hence remains [illegible]). This is achieved by setting signals [illegible] Figure 8) to 0 and signals [illegible] to [illegible]. A field is provided in the [illegible] instruction which is executed on an array element [illegible] whether data is allowed to propagate [illegible] along the bus or is stopped as just described. This [illegible] multiple array elements to load the same data [illegible] different fields of the [illegible] which are [illegible] during the same clock cycle.

[illegible] architecture which [illegible] a rec[illegible] terms of [illegible]

CLA[illegible]

1. [illegible] processor [illegible] comprising:

a plurality of [illegible] each element having at least one input [illegible] at least one output port, each [illegible] having [illegible] data [illegible] valid data signal line; a[illegible]

a [illegible] structure which [illegible] a plurality of switches which are arranged so as to allow [illegible] output port of any first processing element to be connected to the input port of any [illegible] processing element for a time interval;

each processing [illegible] enabled to set a value on the valid data signal line of [illegible] output port to a first logic state [illegible] associated data bus contains [illegible] transfer value and to a second logic state when the data bus does not contain a transfer value;

each processing element being further enabled to enter a waiting state for [illegible] predetermined time interval when the value on the [illegible] line of the associated input port is in the second logic state.

2. A processor [illegible] claim 1, wherein the processing [illegible] programmable in such a way as to set the predetermined time interval.

3. A processor [illegible] claim 1, wherein the processing [illegible] after entering the waiting state [illegible] predetermined time interval, to resume [illegible] data signal line.

4. A processor [illegible] claim 1, 2 or 3, wherein [illegible] further enab[illegible] read data from [illegible] port when the value [illegible] line of the [illegible] state.

5. [illegible] any preceding claim [illegible] input and output ports [illegible] elements [illegible]

[illegible] is less than or equal to the first number.

5. A processor as claimed in claim 4, wherein the second processing element is enabled to load any number of bits less than or equal to the first number of bits.

6. A processor as claimed in any preceding claim, wherein the transfer bus structure at a location in front of each of which the corresponding output port is connected to the bus structure, in the direction of signal flow, is such that, during a transfer bus cycle, the second processing element may set a predetermined logic value on the bus structure.

7. A processor as claimed in claim 6, wherein, in the absence of a driven logic value set on the bus structure by the processing element is enabled to set a predetermined logic value on the bus structure.

8. A processor as claimed in any preceding claim, wherein the processing elements include memory elements for storing received data.

9. A processor as claimed in claim 8, wherein the processing elements include at least one memory element for storing program data.

10. A processor as claimed in any preceding claim, wherein the processing elements include Arithmetic Logic Units.

11. A processor as claimed in any preceding claim, wherein the processing elements include multiplier units.

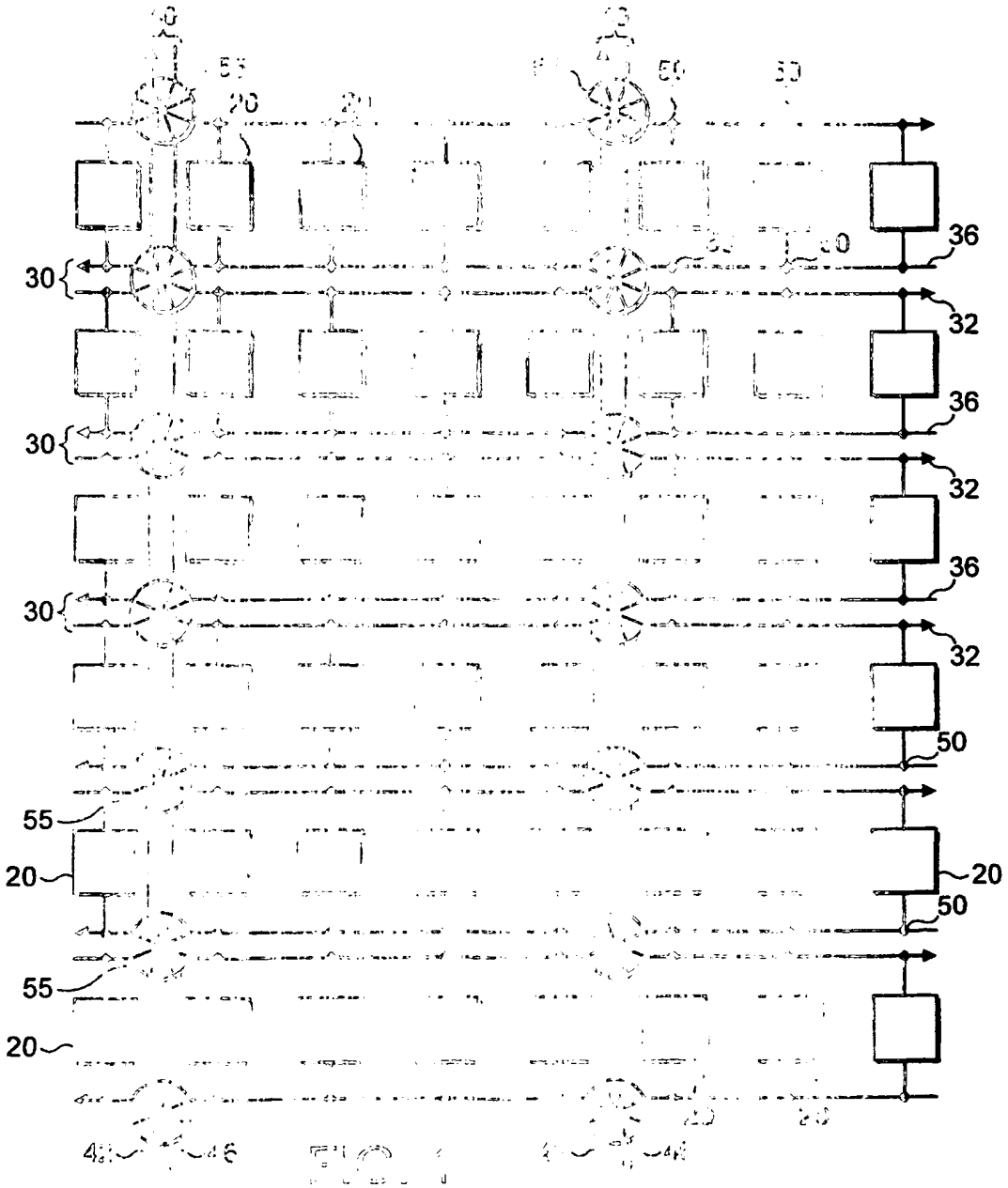
12. A processor as claimed in any preceding claim, [illegible]

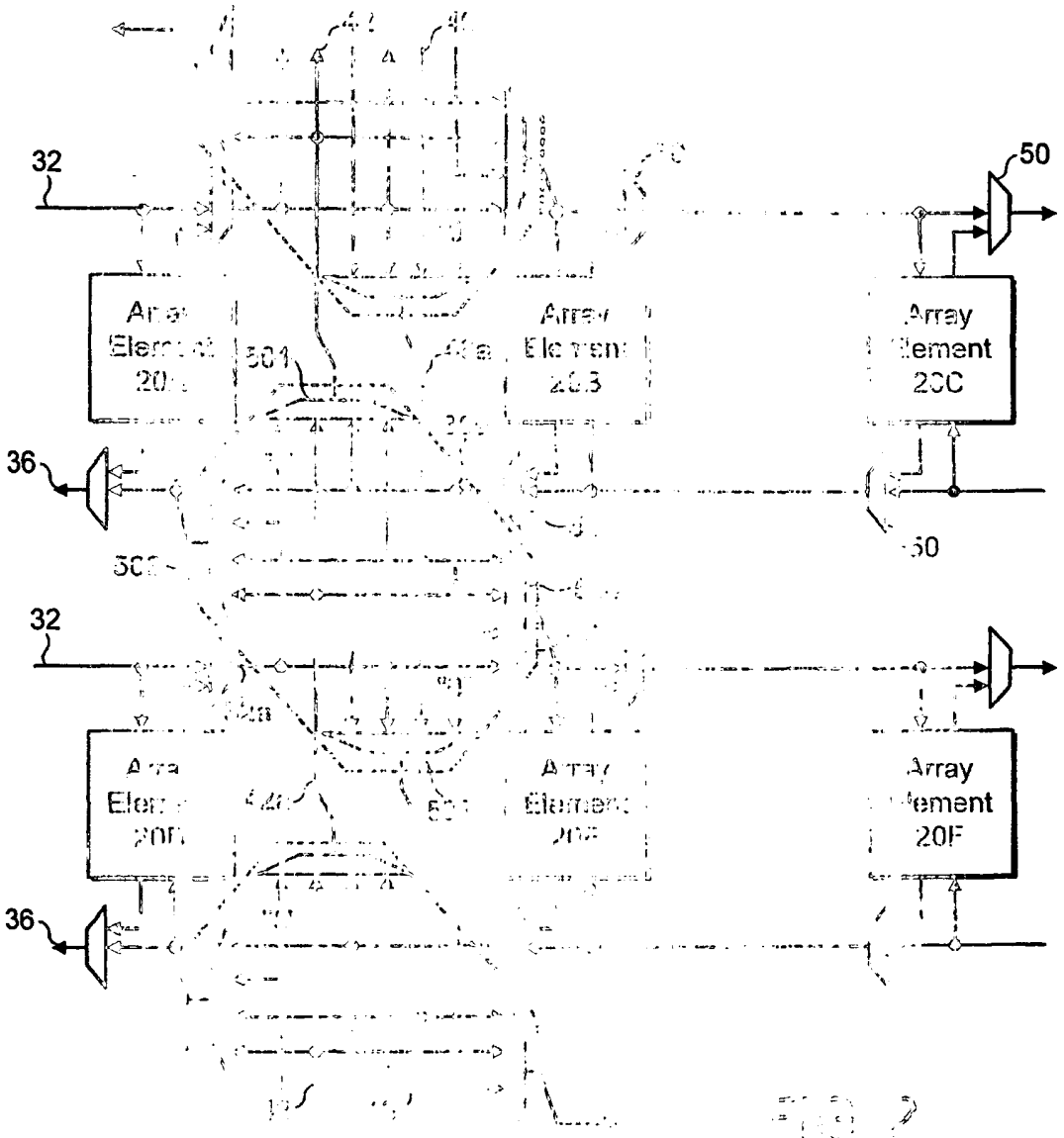
[illegible] first

[illegible] the

5 [illegible]

[illegible] the

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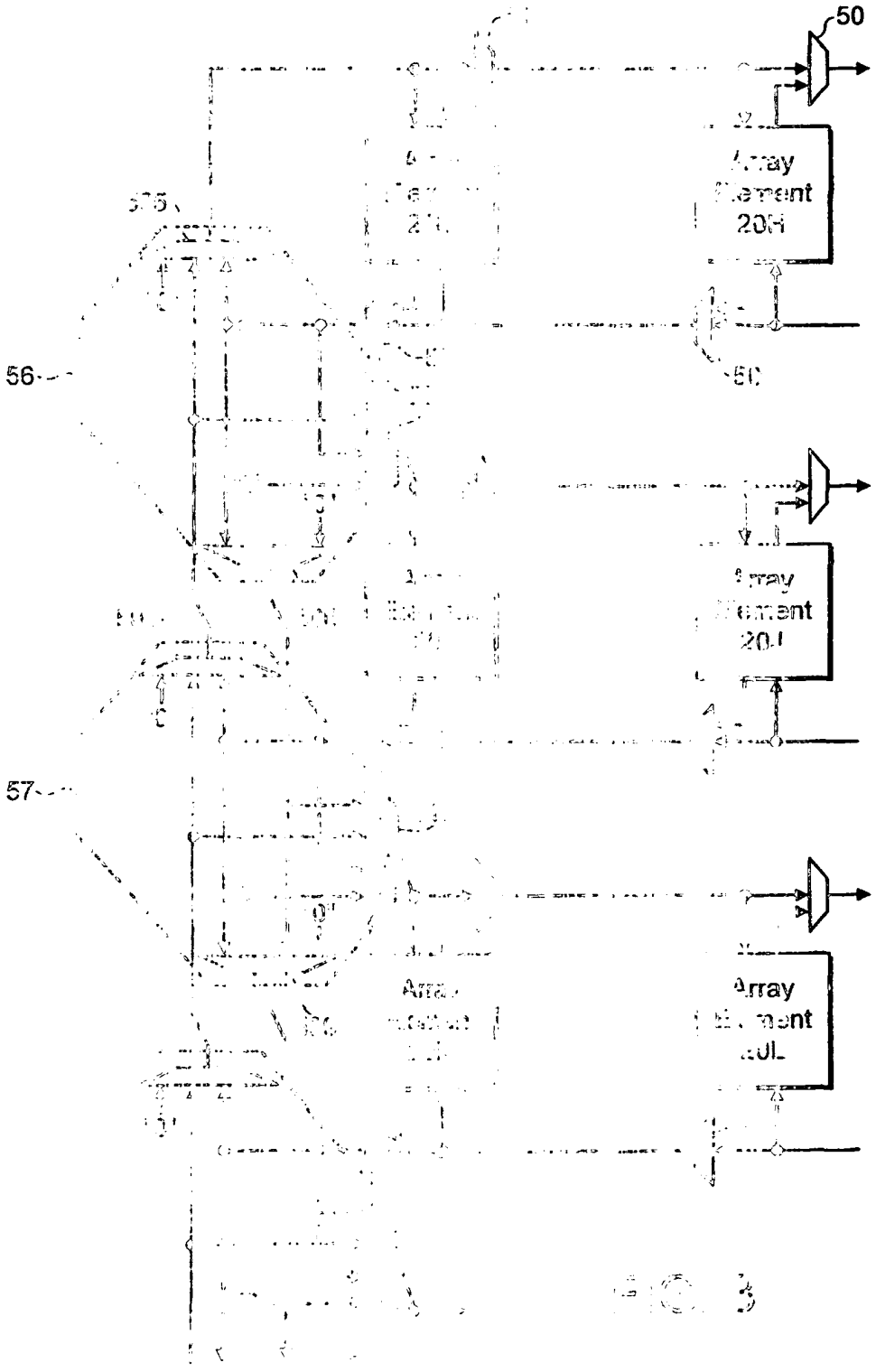
Array Element 20C
36
32
36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Element
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Element
20I
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Array
Element
20L

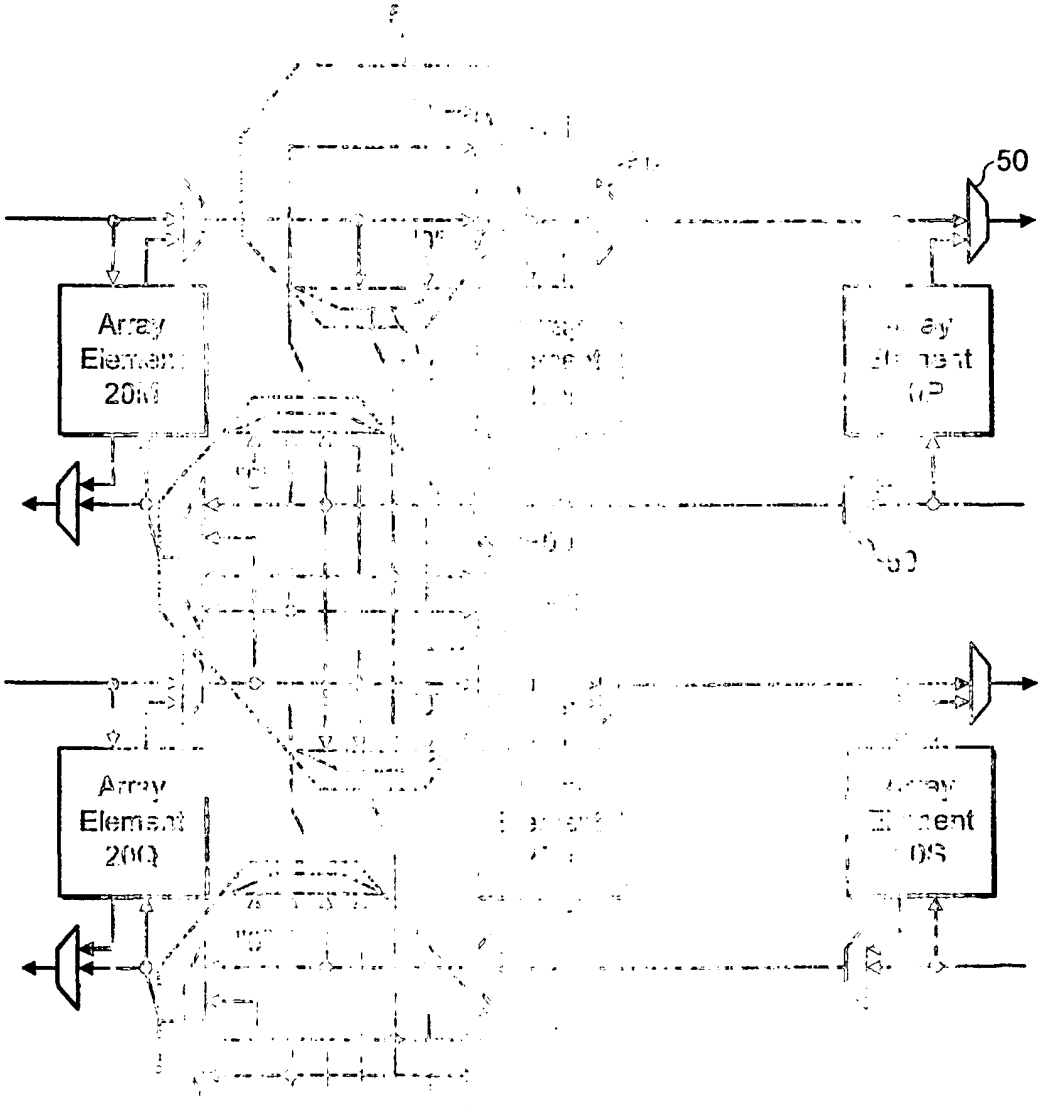


FIG. 4

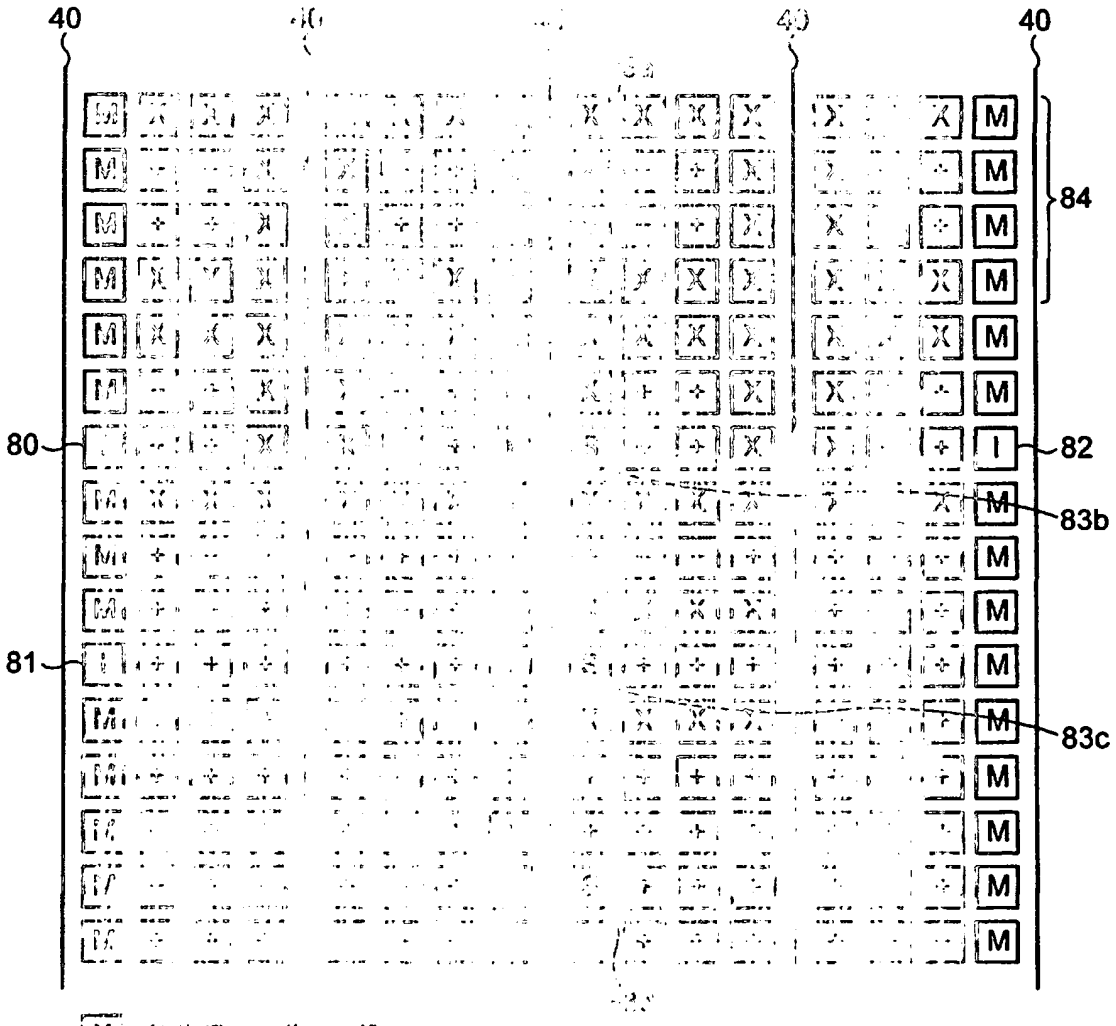
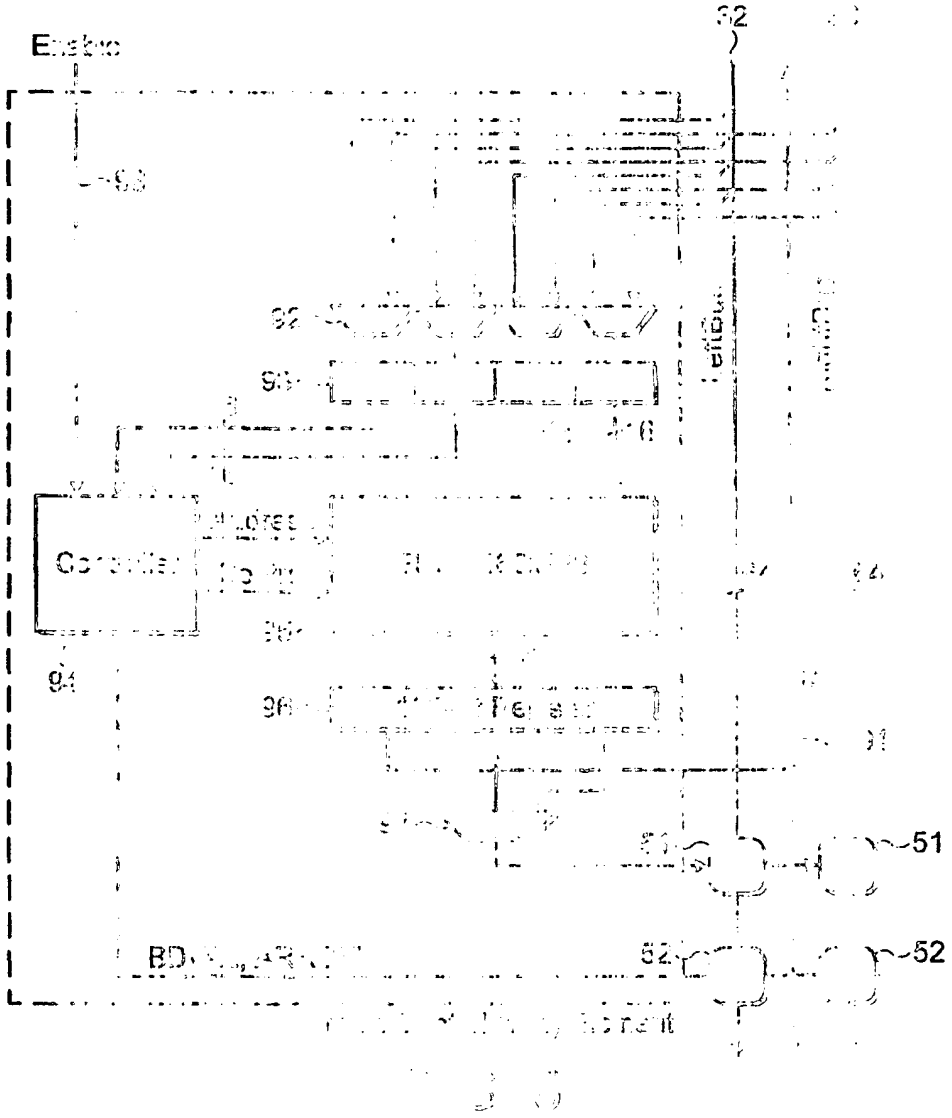


FIG. 8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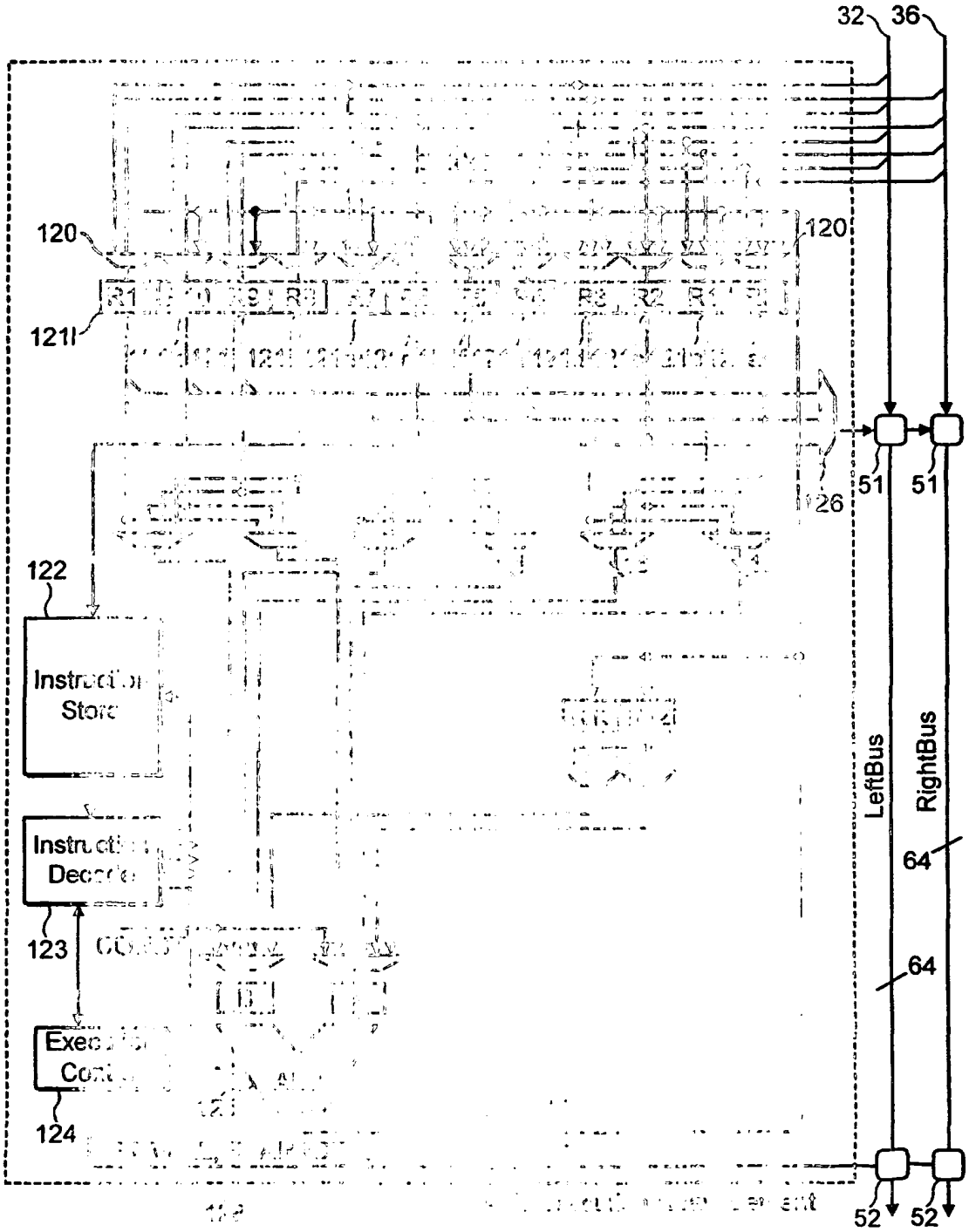
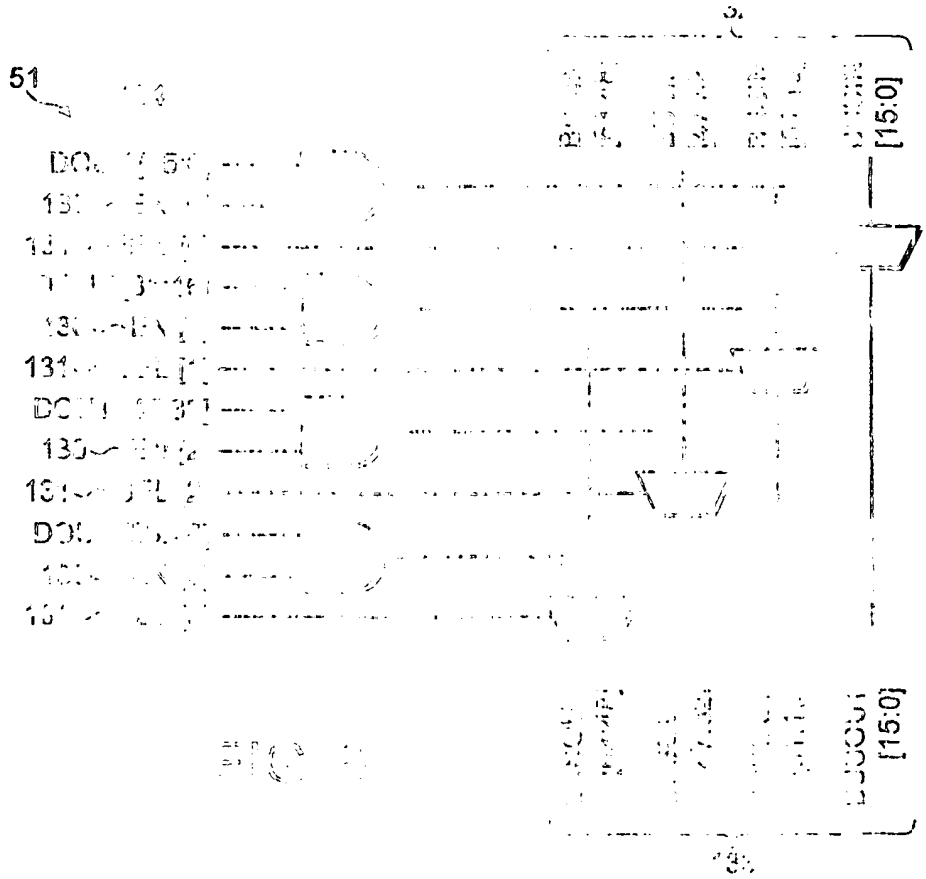

32
36
120
120
121
121
R1
R2
R3
R3
R2
R1
26
51
51
122
Instruction
Store
Instruction
Decode
123
Execute
Control
124
LeftBus
RightBus
64
64
52
52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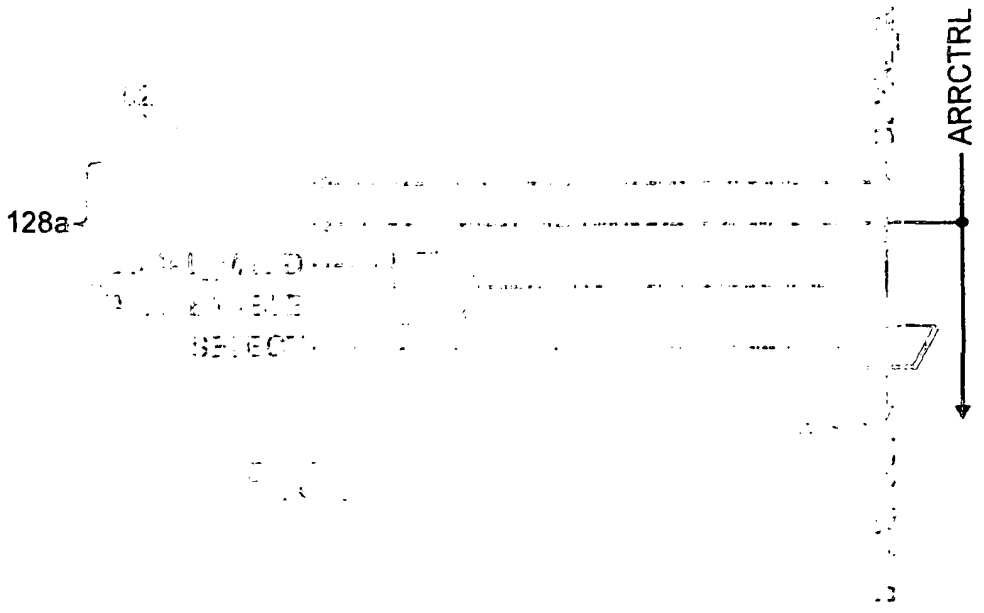
[15:0]
[15:0]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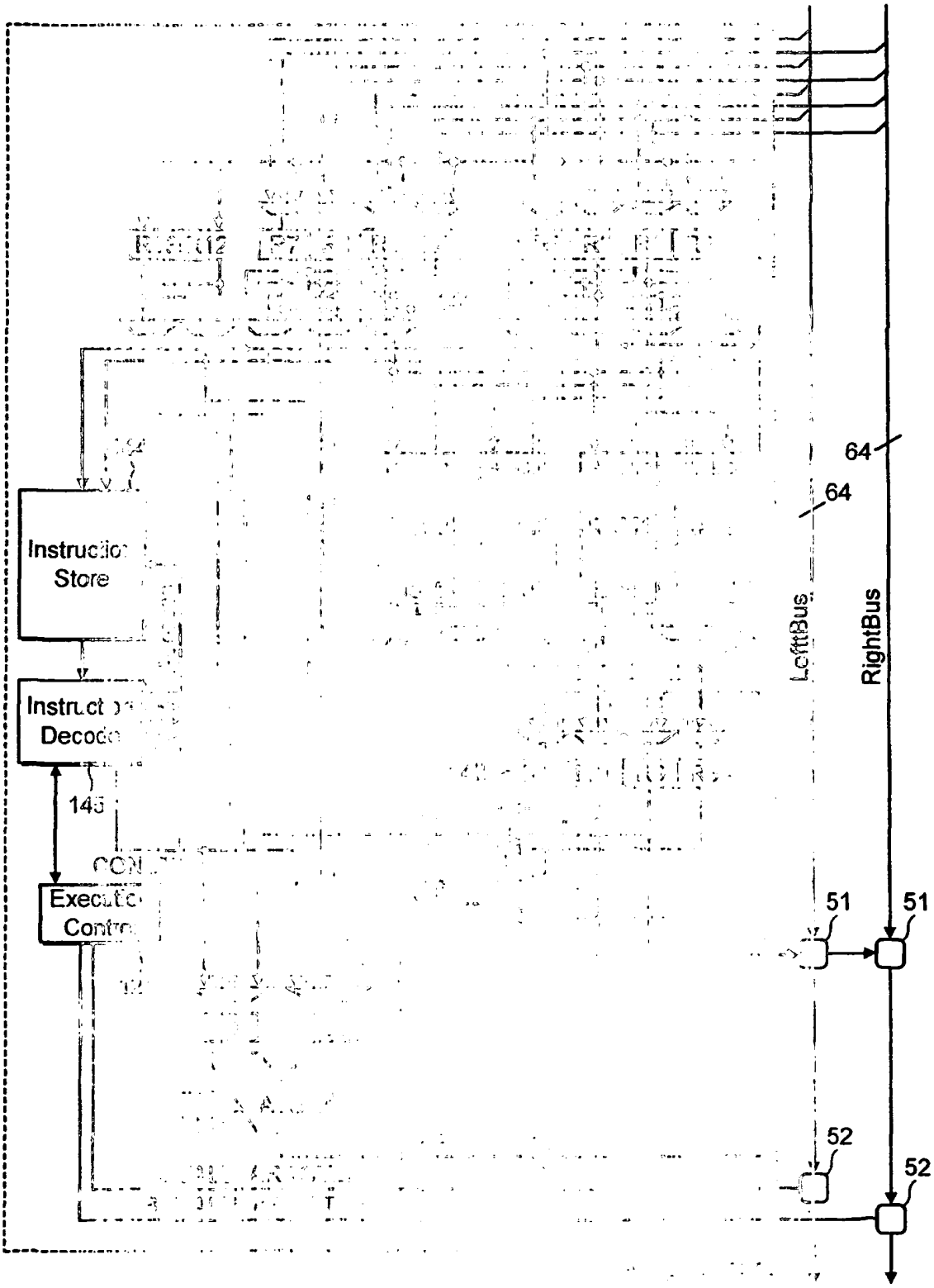
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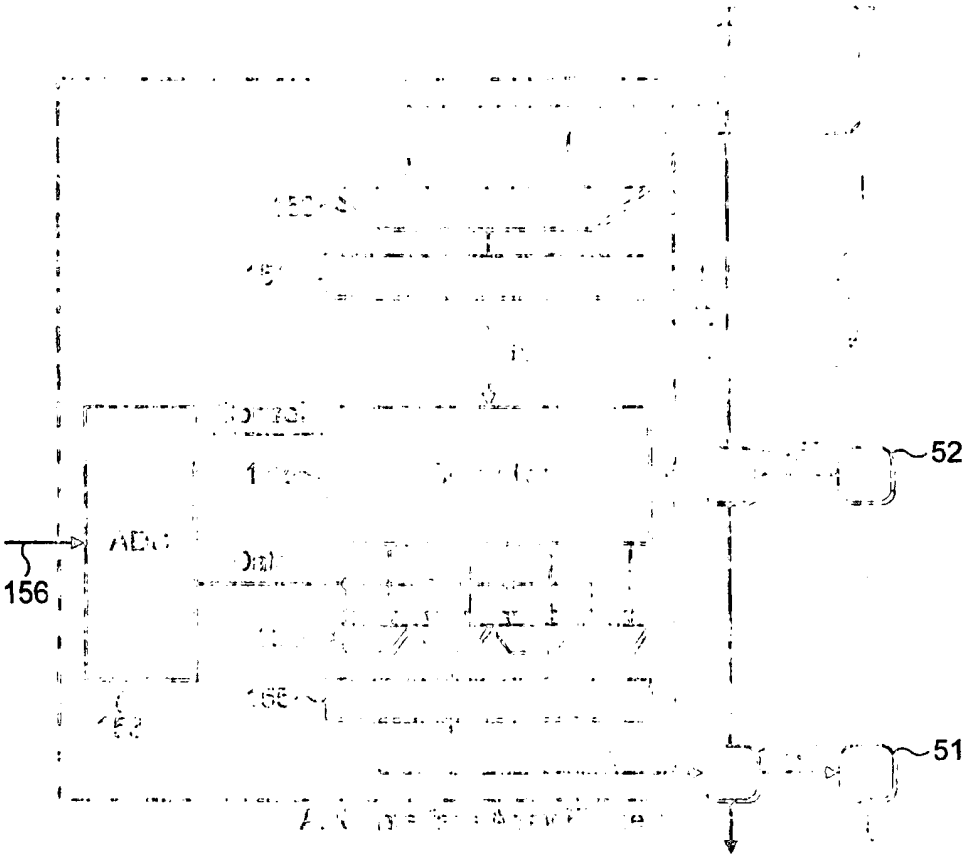
64
Instruction Store
LeftBus
RightBus
145
51
51
52
52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ADDRESS
DATA

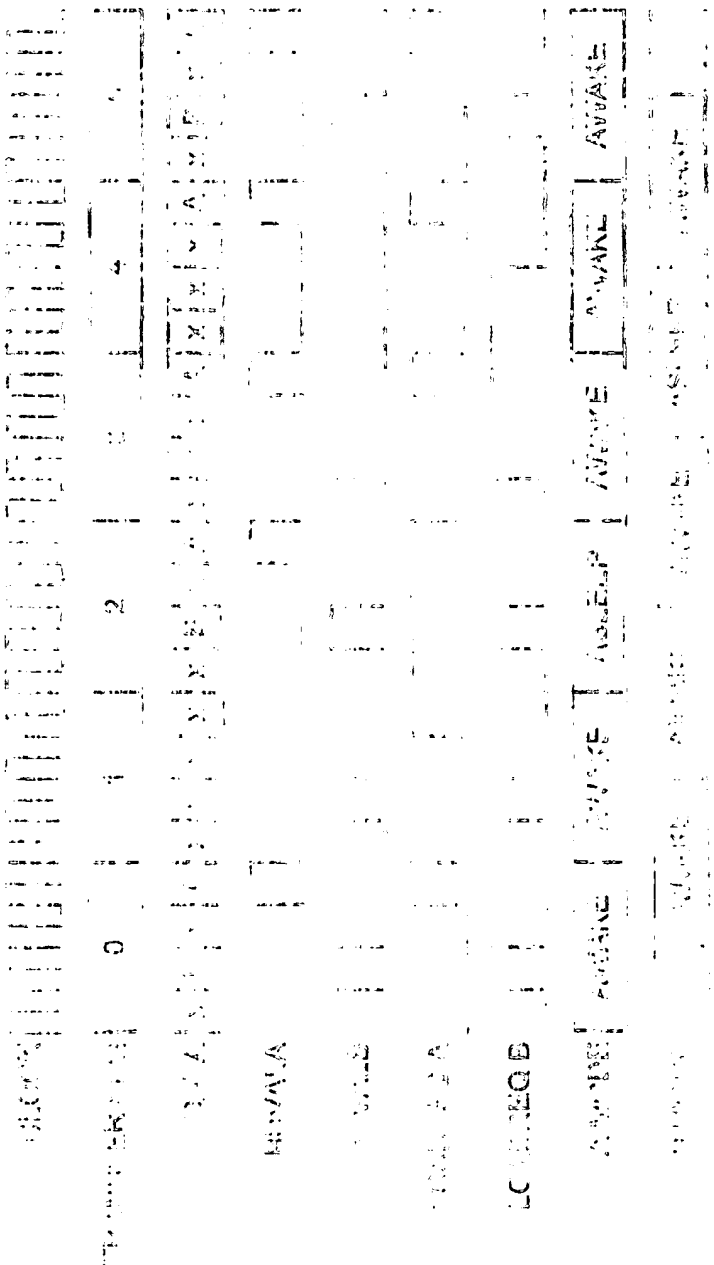

Fig. 10

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ZW

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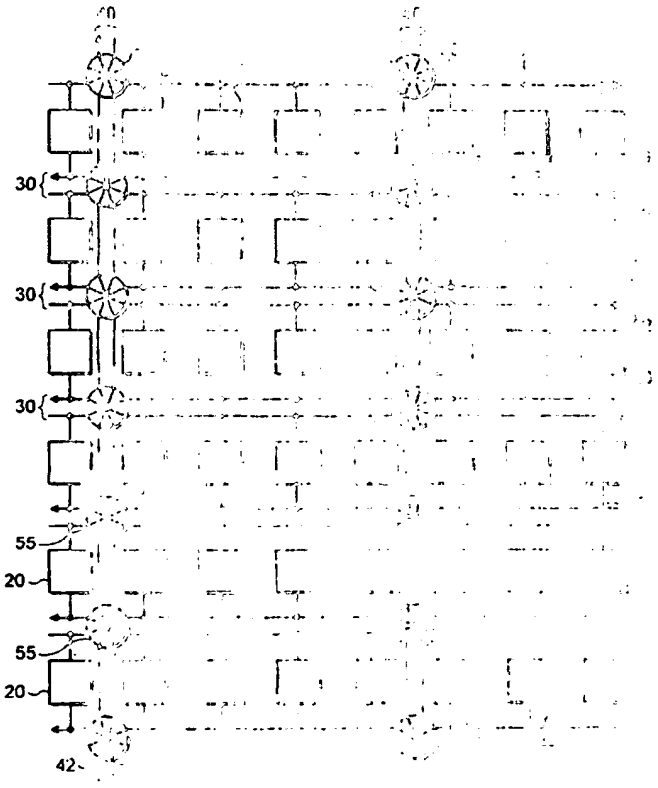
API patent (BF, BJ, CF,
ML, MR, NE, SN, TD,

[Continued on next page]

(54) Title: PROC[illegible] ARCHITE[illegible]



[illegible] There is described a processor [illegible] in a plurality of processing el[illegible] having at least one input [illegible] input port, each port hav[illegible] a valid data signal line; [illegible] which contains a plurality [illegible] arranged so as to allow [illegible] first processing element [illegible] input port of any second [illegible] a time interval, in which [illegible] is enabled to set a value [illegible] line of its output port to [illegible] the associated data bus [illegible], and to a second logic [illegible] does not contain a trans[illegible] each processing element [illegible] a waiting state for a [illegible] interval when the value on [illegible] of the associated input [illegible] gic state. This reduces [illegible] of the device.

WO 02/050700 A3

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[illegible] refer to the "Guid-[illegible] aring at the begin-[illegible]

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A. CLASSIFICATION OF SUBJECT MATTER
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According to International Patent Classification (IPC) [illegible]

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G03

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

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C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	SCHMITT U ET AL: [illegible]	3,4, [illegible]3
A	page 33, left-hand column [illegible] GB, left-hand column [illegible]	5-8

[X] Further documents are listed in the continuation of box C. [ ] See patent family members annex.

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INTERNATIONAL SEARCH REPORT

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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A	SCH[illegible] ET AL: [illegible] PRO[illegible] FOR [illegible] PRO[illegible] THE [illegible] CON[illegible] (IC[illegible]), [illegible], IL, [illegible] 6 - 8, 1999, NEW YORK, IEEE, US, vol. [illegible] (1999-[illegible]), pages [illegible] the whole document	[illegible]-13
A	EP [illegible] 094 A ([illegible]) 19 January 2000 (2000-01-19) page 17, line 2[illegible] - line 3[illegible]; figure [illegible]	1

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